14. The method of claim 13 wherein said data processing further includes a Target Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism should not be polled by said dispatcher and an interrupt given to said processor, said method further comprising overridding said TDI value and driving an immediate interrupt to said processor when said overide bit is in its first condition.

15. The method of claim 13 wherein said main storage is divided into multiple partitions, with each partition having a vector mechanism operable to register I/O requests by said devices to send or receive data from that partition of main storage, each partition having an associated override bit for that partition, and said processor is a hypervisor, said method further comprising setting by said hypervisor the override bit for that partition when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

16. The method of claim 15 wherein said data processing system further includes one or more central processing units (CPUs) assignable by said hypervisor to one or more of said partitions, said method further comprising setting by said hypervisor, the override bit of one partition when that partition does not have a CPU assigned to it.

17. The method of claim 13 further comprising resetting said override bit to its second condition after an interrupt is handled by said processor.

18. The method of claim 17 further comprising resetting said override bit to its second condition upon the first to occur for said interrupt handling or said dispatcher polling.

19. A program product for controlling the transfer of data in a data processing system having a processor handling an I/O request in an I/O operation, main storage controlled by the processor for storing data, and one or more I/O devices for sending data to or receiving data from said main storage, said program product comprising:

a computer readable medium having recorded thereon computer readable program code means for performing the method comprising:

registering in a vector mechanism, I/O requests by said devices to send or receive data from said main storage;

polling with a dispatcher, said vector mechanism to determine if there is an outstanding I/O request; and

sending an immediate interrupt to said processor when an override bit has a first condition for handling an I/O request from said I/O device(s), or polling with said dispatcher, said vector mechanism to determine if there is an outstanding I/O request when said overide bit is in a second condition..

20. The program product of claim 19 wherein said data processing further includes a Target Delay Interval (TDI) register containing a TDI value for determining when the vector mechanism should not be polled by said dispatcher and an interrupt given to said processor, said method further comprising overridding said TDI value and driving an immediate interrupt to said processor when said overide bit is in its first condition.

21. The program product of claim 19 wherein said main storage is divided into multiple partitions, with each partition having a vector mechanism operable to register I/O requests by said devices to send or receive data from that partition of main storage, each partition having an associated override bit for that partition, and said processor is a hypervisor, said method further comprising setting by said hypervisor the override bit for that partition when said hypervisor is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

22. The program product of claim 21 wherein said data processing system further includes one or more central processing units (CPUs) assignable by said hypervisor to one or more of said partitions, said method further comprising setting by said hypervisor, the override bit of one partition when that partition does not have a CPU assigned to it.

23. The program product of claim 19 wherein said method further comprises resetting said override bit to its second condition after an interrupt is handled by said processor.

24. The program product of claim 23 wherein said method further comprises resetting said override bit to its second condition upon the first to occur of said interrupt handling or said dispatcher polling.